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10/759,690	01/16/2004	Richard L. Black	P/10-658	8450

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EXAMINER	
KITOV, ZEEV V	

ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/759,690	BLACK, RICHARD L.	
	Examiner	Art Unit	
	ZEEV KITOV	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 9, 11 - 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 9, 11 - 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on April 14, 2008. Claims 10, 16 – 19 are deleted; Claims 1, 9 and 15 are amended. A new Office Action follows.

IDS

The IDS form submitted on 07/14/05 was approved by the Examiner. However, further analysis indicated that the reference DE 32 02 319 recited in the International Search Report as X-reference was submitted only partially since all the Drawings were missing. As a matter of fact, substantial part of the instant Office Action is based on these Drawings and omission of the Drawings has caused unnecessary burden on Examiner and delay in prosecution. The reference should be resubmitted.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Ichikawa (US 6,285,235). Regarding Claim, 1 Ichikawa discloses a gate control circuit for power switching transistor (Fig. 23) wherein the power switching transistor (1 in Fig. 23) has a control electrode (G) and two main electrodes (E and C), the first main electrode is

coupled to a first terminal (upper plate) of the storage capacitor (6A in Fig. 19), while a second terminal of the storage capacitor is coupled to a reference voltage (negative terminal of the voltage source 2B in Fig. 19). The circuit comprising: a sensing circuit (20, 21, 22 and 3E in Fig. 23 and 15, 17, 18, 3E in Fig. 21) including a protection switch (3E in Fig. 21 and 23) for sensing the rate of change of voltage (dv/dt) by the block 20 in Fig. 23) with respect to time at the first main electrode of the power switching transistor. The sensing circuit senses the rate of change of the voltage between the main electrodes, i.e. at the main electrode (E in Fig. 23) with respect to another electrode (C in Fig. 23). As to a rate of change being proportional to the magnitude of the current flowing through the main electrode, since the transistor current, at least partially, flows through the capacitor (6A in Fig. 19), the dV/dt factor is inherently proportional to the value of the capacitor current (see Electrical Engineering textbooks).

The sensing circuit further controls a protection switch (3E in Fig. 23) to remove a control signal to the control electrode of the power switching transistor (G in Fig. 23) to turn off the power switching transistor (1 in Fig. 23) when the rate of change exceeds a first predetermined value (22 in Fig. 23).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1- 6 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Junge (DE 2,831,495) in view of Klausecker (DE 3,202,319). Regarding Claim 1, Junge discloses the inverter with the power switching transistor (T in Fig. 1) having a control electrode (base) and first and second main electrodes (collector and emitter accordingly), the first main electrode is coupled to the a first terminal of the storage capacitor while the second terminal of the storage capacitor is coupled to a reference potential (negative power supply line). According to Junge (see Abstract), the switch is used to protect the storage capacitor against the surge currents.

However, Junge does not disclose a control circuit for controlling the power switching transistor (LT in Fig. 5). Klausecker discloses the circuit controlling the switching transistor including a sensing circuit (C, R, Th in Fig. 5), including a protection switch (Th in Fig. 5), and sensing the rate of change of voltage with respect to a time at the first main electrode (drain) of the power switching transistor. As to the rate of change of voltage being proportional to the magnitude of the current flowing through the first main electrode, this requirement is satisfied since the current value in the capacitor (C in Fig. 5) is proportional to the rate of change of the voltage across the capacitor and since the bottom plate of the capacitor has a fixed potential value, the voltage across the capacitor depends exclusively on the drain voltage of the power transistor. Therefore, the rate of change (dV/dt) is detected by the sensor circuit (C, R in Fig. 5). The sensing circuit controls the protection switch (transistor Th in Fig. 5) to remove a control signal to the control electrode (gate G in Fig. 5) of the power switching transistor when the rate of change of the drain voltage is such that it causes the capacitor current

through the resistor (R in Fig. 5) and a zener diode (Z in Fig. 5) to get a sufficient value to switch on the transistor (Th in Fig. 5) thus removing the a control signal from the gate of the power transistor (LT in Fig. 5), when the rate of change and the current exceeds a first predefined value, i.e. minimal base current of the transistor (Th in Fig. 5) necessary to switch the transistor out from a cut-off regime.

Therefore, (I) Junge discloses a problem of protection of the storage capacitors against surges and the method of protection by switching the power transistor, (II) Ishikawa provides a detailed circuit solution for the problem of sensing and switching the power transistor since his dynamic sensor distinguishes between steady over-currents and the surges currents. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the detection and switching solution of Klausecker to protect the storage capacitor of Junge against the surges, since when the problem is recognized and the solution is known, a person of ordinary skill in the art would have been motivated to combine the prior art to achieve the claimed invention and that there would have been a reasonable expectation of success. A motivation for such combination would be to achieve better protection of the storage capacitor.

Regarding Claims 2 and 5, Klausecker discloses the sensing circuit including a capacitor (C in Fig. 5) coupled to a main electrode (drain) of the power switching transistor and a resistor (R in Fig. 5) coupled to receive a pulse of current from said capacitor (R in Fig. 5). A sensed voltage in form of a current develops a voltage drop across the emitter-base junction of the protection switch (transistor Th in Fig. 5) such that a voltage sensed turns on the protection switch. As to the protection switch being

turned on if the voltage across the resistor exceeds a second predefined value, i.e. minimal emitter-base voltage (normally, about 0.5 – 0.6 V), Klausecker further shows another version of the protection transistor activation (Fig. 3), wherein the resistive divider (Rb, Rr in Fig. 3) is formed. A voltage drop across the bottom resistor (Rr in Fig. 3) should have a sufficient value to switch the protection transistor from its cut-off regime. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Fig. 5 of Klasecker according to details of Fig. 3 of Klausecker, i.e. by introducing a voltage divider, since such arrangement helps to adjust a value of switching threshold.

Regarding Claims 3, 4, 11 and 12, Klasecker discloses the protection switch as being a bipolar junction transistor.

Regarding Claim 6, Klausecker discloses a diode (Z in Fig. 5) coupled across the base-emitter junction of the protection transistor to discharge the capacitor (C in Fig. 5).

Regarding Claims 8 and 14, Klausecker discloses the circuit with the power switching transistor being a field effect transistor (LT in Fig. 5).

As per Claims 9 and 15, they differ from Claims 1 and 2 rejected above by their limitations regarding details a sensing resistor and sensing capacitor connections. In the Junge circuit modified according to teachings of Klausecker, a sensing capacitor (C in Fig. 5 of Klausecker) has first and second terminals, the first terminal is coupled to the first main electrode of the power switching transistor and the storage capacitor (connected to collector of the transistor (T in Fig. 1 of Junge), the sensing capacitor generates a current representative of the rate of change of voltage of the power

transistor main terminal (collector or drain) with respect to time across the storage capacitor, since the bottom plate of the storage capacitor has a fixed potential, the change of voltage at the first main terminal of the power switching transistor coincide with the change of voltage across the storage capacitor; and

a sensing resistor (Rr in Fig. 3 of Klausecker) having first and second terminals, the first terminal of the sensing resistor coupled to the reference potential, and the second terminal of the sensing resistor coupled to both the control electrode of the protection transistor (base of transistor T2 in Fig. 3) and the second terminal of the sensing capacitor (C in Fig. 5), the sensing capacitor providing a current to the sensing resistor to develop a sensing voltage across the sensing resistor to turn on the protection transistor if the sensing voltage across the sensing resistor (Rr in Fig. 3) exceeds a predefined sensing voltage value, i.e. about 0.5 – 0.6 V necessary to move the protection transistor from the cut-off regime to an active regime. A motivation for merging the circuits Fig. 3 and Fig. 5 of Klausecker was recited above (see Claims 2 and 5 rejections above). The protection transistor of Klausecker is adapted to remove a control signal to the control electrode of the power switching transistor (gate G in Fig. 5) to turn off the power switching transistor (LT in Fig. 5) if the rate of change of voltage with respect to time across the storage capacitor exceeds a first predefined rate of change value, i.e. when the current in capacitor (C in Fig. 5) is strong enough to cause a voltage drop across resistor (Rr in Fig. 3) sufficient to move the protection transistor (Th in Fig. 5) from the cut-off regime to an active or saturation regime.

Claims 7 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Junge in view of Klausecker and Ohura et al. (US 5,818,281). Regarding claim 7 Junge and Klausecker disclose all the elements of previous Claims but do not teach the protection switch comprising a field effect transistor JFET. Ohura et al. teaches a protection circuit wherein the protection switch is a FET (Fig. 5 element 2). It would have been obvious to a person with the skill in the art at the time the invention was made to modify the Junge circuit according to the teachings of Ohura et al. because it allows a higher switching speed (col. 1 lines 12 - 16). Additionally, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the BJT element by its FET equivalent, because the substitution of one known element for another, which is its functional equivalent, would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Response to Arguments

Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836